AMENDMENTS TO THE CLAIMS:

Listing of claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1-11. (Canceled)

12. (New): A semiconductor device manufacturing method comprising the steps of:

forming a lower resist layer on a patterning objective layer;

forming an organic intermediate layer made of organic silicon-containing material, having no Si-O bond in its structure, on the lower resist layer;

forming an upper resist layer made of alicyclic resin on the organic intermediate layer;

forming a pattern by exposing/developing the upper resist layer;

transferring the pattern of the upper resist layer onto the organic intermediate layer by etching the organic intermediate layer selectively with respect to the lower layer while using the upper resist layer as a mask;

transferring a pattern of the organic intermediate layer onto the lower resist layer by etching the lower resist layer while using the organic intermediate layer as a mask; and

patterning the patterning objective layer by etching the patterning objective layer while using the lower resist layer and the organic intermediate layer as a mask.

13. (New): A semiconductor device manufacturing method comprising the steps of:

forming a lower resist layer on a patterning objective layer;

forming an organic intermediate layer made of organic silicon-containing material, having no Si-O bond in its structure, on the lower resist layer;

forming an upper resist layer made of alicyclic resin on the organic intermediate layer;

forming a pattern by exposing/developing the upper resist layer;

transferring the pattern of the upper resist layer onto the organic intermediate layer by etching the organic intermediate layer while using the upper resist layer as a mask;

transferring a pattern of the organic intermediate layer onto the lower resist layer by etching the lower resist layer while using the organic intermediate layer as a mask; and

patterning the patterning objective layer by etching the patterning objective layer while using the lower resist layer and the organic intermediate layer as a mask, and the organic intermediate layer is etched simultaneously with etching of the patterning object laver.

14. (New): A semiconductor device manufacturing method comprising the steps of:

forming a lower resist layer on a patterning objective layer;

forming an organic intermediate layer made of organic silicon-containing material, having no Si-O bond in its structure, on the lower resist layer;

forming an upper resist layer made of alicylic resin on the organic intermediate layer;

forming a pattern by exposing/developing the upper resist layer;

transferring the pattern of the upper resist layer onto the organic intermediate layer by etching the organic intermediate layer while using the upper resist layer as a mask;

transferring a pattern of the organic intermediate layer onto the lower resist layer by etching the lower resist layer while using the organic intermediate layer as a mask, and simultaneously the upper resist layer is etched and removed; and

patterning the patterning objective layer by etching the patterning objective layer while using the lower resist layer and the organic intermediate layer as a mask.

15. (New): A semiconductor device manufacturing method comprising the steps of:

forming a lower resist layer on a patterning objective layer, the lower resist layer which is thicker than a thickness of the patterning objective layer;

forming an organic intermediate layer made of organic silicon-containing material, having no Si-O bond in its structure, on the lower resist layer;

forming an upper resist layer made of alicylic resin on the organic intermediate layer;

forming a pattern by exposing/developing the upper resist layer;

transferring the pattern of the upper resist layer onto the organic intermediate layer by etching the organic intermediate layer while using the upper resist layer as a mask;

transferring a pattern of the organic intermediate layer onto the lower resist layer by etching the lower resist layer while using the organic intermediate layer as a mask; and

patterning the patterning objective layer by etching the patterning objective layer while using the lower resist layer and the organic intermediate layer as a mask.

16. (New): A semiconductor device manufacturing method according to claim 12,

wherein silicon contained in the organic intermediate layer is bonded only to at least one of hydrogen, carbon, and silicon.

17. (New): A semiconductor device manufacturing method according to claim 13, wherein silicon contained in the organic intermediate layer is bonded only to at least one of hydrogen, carbon, and silicon.

18. (New): A semiconductor device manufacturing method according to claim 14, wherein silicon contained in the organic intermediate layer is bonded only to at least one of hydrogen, carbon, and silicon.

19. (New): A semiconductor device manufacturing method according to claim 15, wherein silicon contained in the organic intermediate layer is bonded only to at least one of hydrogen, carbon, and silicon.

20. (New) : A semiconductor device manufacturing method according to claim 12, wherein the upper resist is exposed by an ArF excimer laser.

21. (New): A semiconductor device manufacturing method according to claim 13, wherein the upper resist is exposed by an ArF excimer laser.

22. (New): A semiconductor device manufacturing method according to claim 14,

wherein the upper resist is exposed by an ArF excimer laser.

23. (New): A semiconductor device manufacturing method according to claim 15, wherein the upper resist is exposed by an ArF excimer laser.

24. (New): A semiconductor device manufacturing method according to claim 12, wherein the patterning objective layer is formed of a silicon layer, a silicon oxide layer, or silicon nitride layer.

25. (New): A semiconductor device manufacturing method according to claim 13, wherein the patterning objective layer is formed of a silicon layer, a silicon oxide layer, or silicon nitride layer.

26. (New): A semiconductor device manufacturing method according to claim 14, wherein the patterning objective layer is formed of a silicon layer, a silicon oxide layer, or silicon nitride layer.

27. (New): A semiconductor device manufacturing method according to claim 15, wherein the patterning objective layer is formed of a silicon layer, a silicon oxide layer, or silicon nitride layer.

28. (New): A semiconductor device manufacturing method according to claim 12, wherein

the patterning objective layer is a layer on a surface of which an Si-O bond is present, and the lower resist layer is formed of one of aromatic resin, polyvinylphenol resin, and novolac resin.

29. (New): A semiconductor device manufacturing method according to claim 13, wherein the patterning objective layer is a layer on a surface of which as Si-O bond is present, and the lower resist layer is formed of one of aromatic resin, polyvinylphenol resin, and novolac resin.

30. (New): A semiconductor device manufacturing method according to claim 14, wherein the patterning objective layer is a layer on a surface of which an Si-O bond is present, and the lower resist layer is formed of one of aromatic resin, polyvinylphenol resin, and novolac resin.

31. (New): A semiconductor device manufacturing method according to claim 15, wherein the patterning objective layer is a layer on a surface of which an Si-O bond is present, and the lower resist layer is formed of one of aromatic resin, polyvinylphenol resin, and novolac resin.